IN THE CLAIMS

Please amend claim 47 as set forth below.

1. (Previously Presented) An integrated circuit, comprising:

a low resistivity semiconductor substrate having a dielectric region formed therein, a trench defined in the dielectric region and including dielectric sidewalls, and an adjacent cavity defined at least partially by the substrate; and

an electroplated conductive material disposed within the trench to produce an inductance having sides and a bottom, the sides of the inductance being bounded by the dielectric sidewalls and the cavity being adjacent the bottom.

2. (Original) The integrated circuit of claim 1, wherein the dielectric region includes a cap layer formed at a top surface of the semiconductor substrate and the cavity

extends from the cap layer to a bottom surface of the dielectric region.

3. (Original) The integrated circuit of claim 1, wherein a bottom surface of the semiconductor substrate defines a first recessed region underlying the dielectric region.

4. (Original) The integrated circuit of claim 1, wherein the conductive material includes copper.

5. (Original) The integrated circuit of claim 1, wherein the conductive material is disposed within the trench to a depth of at least five micrometers.

6. (Original) The integrated circuit of claim 1, wherein the dielectric region is formed with a silicon based dielectric.

7. (Original) The integrated circuit of claim 1, wherein the dielectric region is formed at a top surface of the

semiconductor substrate, further comprising an active device formed at the top surface.

Claims 8-27 (Canceled)

28. (Previously Presented) A semiconductor device, comprising:

a low resistivity semiconductor substrate having a dielectric region formed therein with a cavity adjacent the dielectric region;

a first inductor of electroplated conductive material formed within a trench defined by the dielectric region, a bottom of the inductor being positioned adjacent the cavity; and

a second inductor of electroplated conductive material overlying the first inductor.

29. (Original) The semiconductor device of claim 28, further comprising a transistor formed at a top surface of the semiconductor substrate.

30. (Original) The semiconductor device of claim 29, wherein a portion of the first inductor is formed below the top surface.

31. (Original) The semiconductor device of claim 28, wherein the first inductor is formed to a thickness of at least five micrometers.

32. (Original) The semiconductor device of claim 31, wherein the second inductor is formed to a thickness of at least five micrometers.

33. (Original) The semiconductor device of claim 28, further comprising a dielectric layer formed between the first and second inductors.

Claims 34-36 (canceled)

37. (Previously Presented) An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

a trench formed in the dielectric region and including side-walls defined by low dielectric constant material; and

high conductivity electroplated material in the trench and defining at least a portion of a passive electronic component.

38. (Previously Presented) An integrated circuit as claimed in claim 37 wherein the low dielectric constant material includes dielectric material defining an array of cavities therein, the dielectric material having a first dielectric constant and the cavities providing a second dielectric

constant lower than the first dielectric constant to form an effective dielectric constant lower than the first dielectric constant.

39. (Previously Presented) An integrated circuit as claimed in claim 38 wherein the dielectric material and the array of cavities produce an effective dielectric constant at least ten percent lower than the first dielectric constant.

40. (Previously Presented) An integrated circuit as claimed in claim 39 wherein the effective dielectric constant is approximately 2.5.

41. (Previously Presented) An integrated circuit as claimed in claim 37 wherein the high conductivity electroplated material includes copper.

42. (Previously Presented) An integrated circuit as claimed in claim 37 wherein the trench is elongated and formed in the shape of an inductance.

43. (Previously Presented) An integrated circuit as claimed in claim 37 and further including a cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity, electroplated material in the trench.

44. (Previously Presented) An integrated circuit as claimed in claim 43 and further including a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity.

45. (Previously Presented) An integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

at least one active component positioned in the active region;

an elongated trench formed in the dielectric region and including side-walls defined by low dielectric constant material;

high conductivity material in the trench and defining at least a portion of an inductive component; and

a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench.

46. (Previously Presented) An integrated circuit as claimed in claim 45 wherein the sealed cavity is sealed by a die attach pad with a pedestal formed on a surface thereof, the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity.

47. (Currently Amended) An integrated circuit as claimed in claim [[45]] 46 wherein the cavity defines a distance between the lower portion of the high conductivity material and the pedestal of approximately one hundred micrometers.

48. (Previously Presented) An integrated circuit as claimed in claim 45 wherein the low dielectric constant material of the side-walls has an effective dielectric constant of approximately 2.5.

49. (Previously Presented) An intermediate component in the formation of an integrated circuit comprising:

a low resistivity, semiconductor substrate including an active region and a dielectric region;

a trench formed in the dielectric region and including side-walls of low dielectric constant material and a bottom defined by the low resistivity, semiconductor substrate, an exterior surface of the bottom being an electroplating contact for electroplating in the trench; and

high conductivity material electroplated in the trench and defining at least a portion of a passive electronic component.

50. (Previously Presented) An integrated circuit as claimed in claim 49 wherein the low dielectric constant material has an effective dielectric constant of approximately 2.5.

51. (Previously Presented) An integrated circuit as claimed in claim 49 wherein the high conductivity material includes copper.